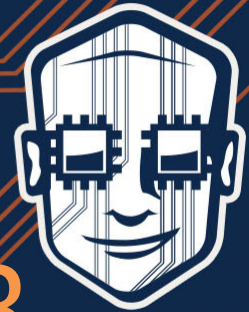


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# HIGH-SPEED LOW-POWER ON-CHIP GLOBAL SIGNALING DESIGN OVERVIEW

Xi Chen, John Wilson, John Poulton,  
Rizwan Bashirullah, Tom Gray

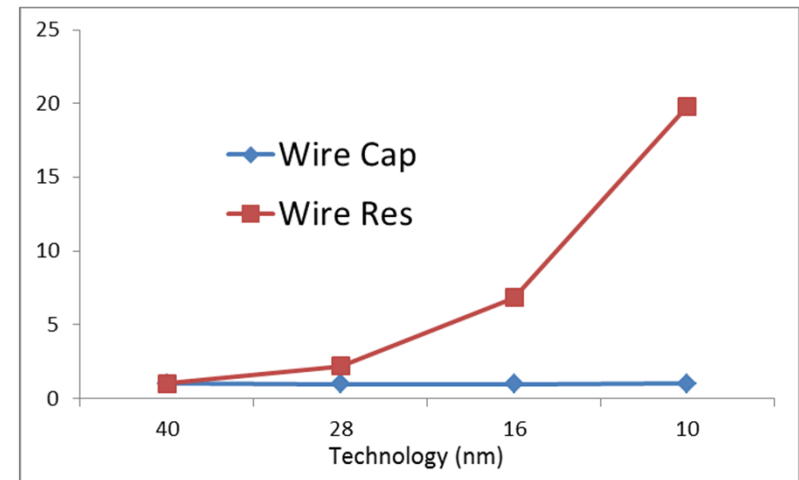


## Agenda

- Problems of On-chip Global Signaling
- Channel Design Considerations
- Multi-hop Serial-links: Repeater and Clocking
- Power Supply Noise Impact
- Circuit Design Considerations
- Conclusion

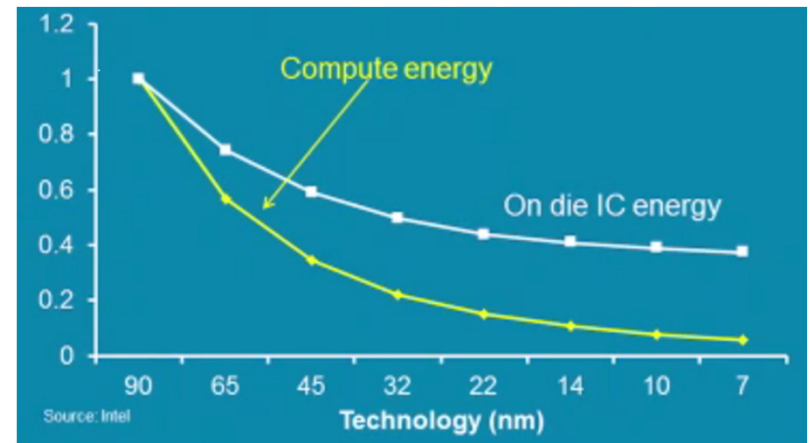
## Problems of Process Shrinking

- When transistors shrink, so do the routing wires...
  - Wire resistance increases exponentially over every process node.
  - Surface scattering & grain boundary scattering are causing wire resistance to increase further for wires < 100nm thick.
- However, communication distances continue to increase...
  - Chip size is staying about constant, but it is more units of 'lambda'.



## Impact on Global Signaling

- Consequences to global signaling:
  - Need larger metal area for the same bandwidth, counteracting the benefit we got from process shrinking...usually solved by adding more routing layers.
  - Energy wise, communication is already more expensive than computation;
  - Latency in global signaling increases dramatically, even with more repeaters.



## On-chip Data Link Techniques

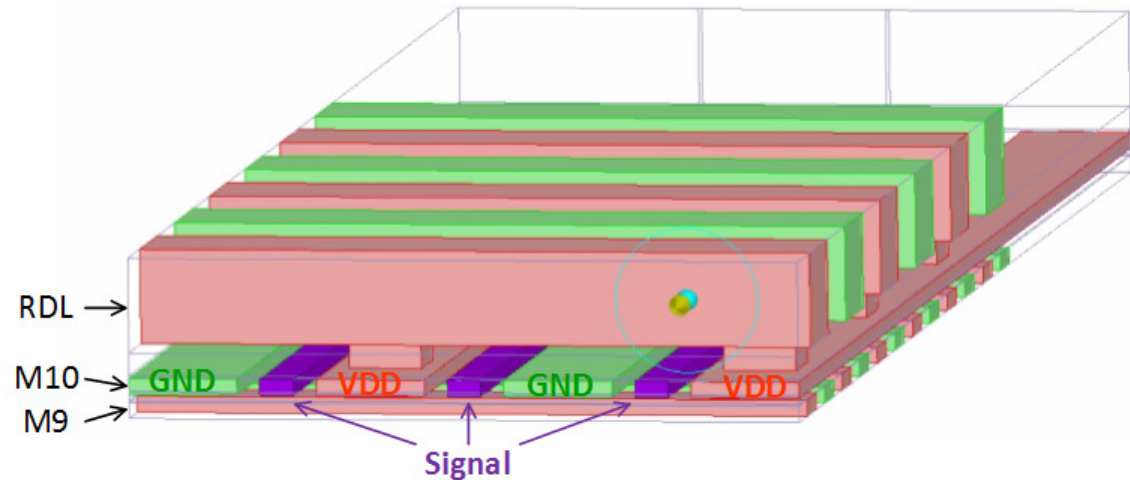
- Bundled-data wiring channels (Fabrics)
  - ~1-2X system clock, Custom designed repeater/re-timer placement, Fully reserved channels for routing, Push the performance of CMOS signaling to its limit.
  - Cannot stop the trend of increasing area & latency, consumes too much resources.
- High-speed Serial-link
  - 8-10X system clock, Low-swing signaling with equalization, Custom designed high-speed channel based on “thick metal”.
  - Unlike off-chip data link, on-chip high-speed serial-link has to work within a digital environment...

## Challenges of On-chip Serial-link

- Channel
  - On-chip metal has much higher resistance compared to package/PCB.
- Power Supply
  - When only logic VDD is available: very limited voltage headroom, large variation.
- Circuit
  - Power efficiency: need about 10s of fJ/bit/mm...for everything
  - Robustness: process variation is significant, and calibration could be expensive.

## On-chip Channels: Metallization

- Building channels on thick metal layers
  - Thicker metal of the upper layers enables longer distances between repeaters.
  - Routing within the framework of existing power delivery network, which can be used as return-paths and cross-talk shields.



## Channel Design Considerations

- Performance of different metal layer options:
  - Bandwidth of RC-dominated channel decreases quadratically with channel length.
  - Thicker metal layer provides longer distance-per-hop @ certain bandwidth, and lower energy & delay per-mm.
  - Therefore, thicker is usually better if available...until Cross-talk hurts.

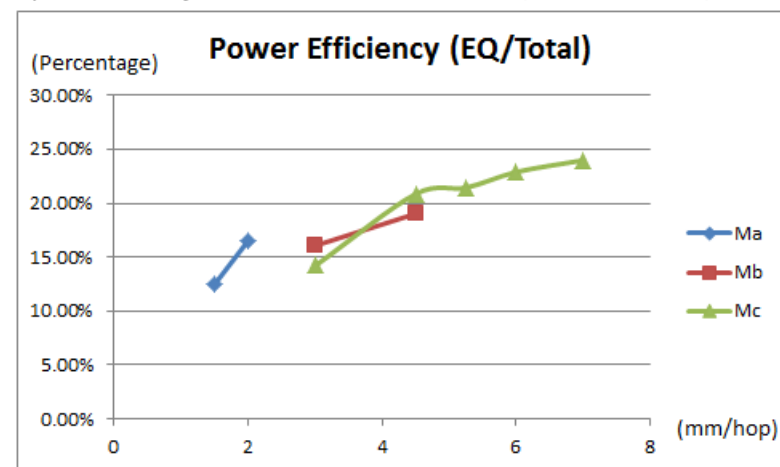
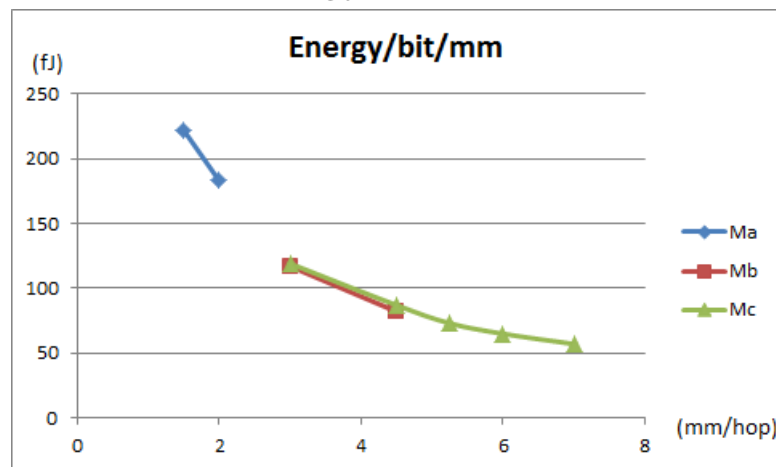
Metal Layer Options	Thickness (normalized)	Signal Width/Space	P/G Shield Width	Signal Pitch	Max Length @ 16Gbps
Ma	1x	0.5 $\mu$ m	3.0 $\mu$ m	4.5 $\mu$ m	2mm
Mb	1.7x	0.8 $\mu$ m	3.6 $\mu$ m	6.0 $\mu$ m	5mm
Mc	2.5x	1.2 $\mu$ m	3.6 $\mu$ m	7.2 $\mu$ m	6.5mm

(100mV signal swing, 0.9V power supply)



## Channel Design Considerations (cont.)

- Experimental results:
  - Longer channel needs more energy for equalization, but the total efficiency increases because the circuit energy is averaged out.
  - Circuit energy overhead can be reduced by shifting to smaller node (ex. 16nm)



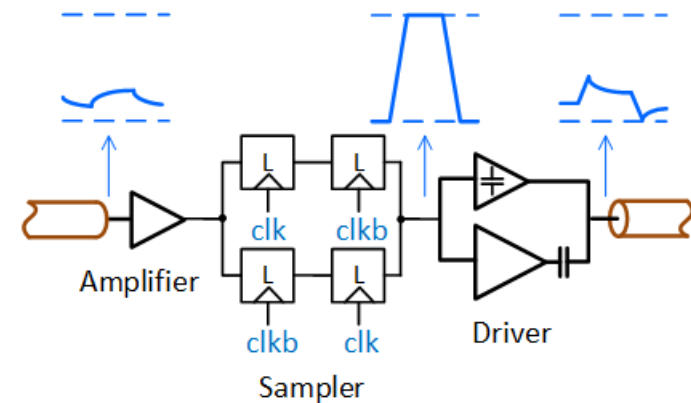
(16 data lanes + 2 clock lanes, 7 hops, 28nm technology, 16Gbps, 900mV supply)

## Multi-hop Serial-link Structure

- Serial-link with repeaters
  - Re-driving: Edge-Rate and Signal-Swing attenuate rapidly on high-resistivity wire, needs re-driving every several mms.
  - Re-timing: Align to reference clock periodically to reduce jitter accumulation.
- Source-synchronous clocking
  - Uses intrinsic delay matching between clock and data lanes;
  - Provides much higher data rates compared to fully synchronous clocking.

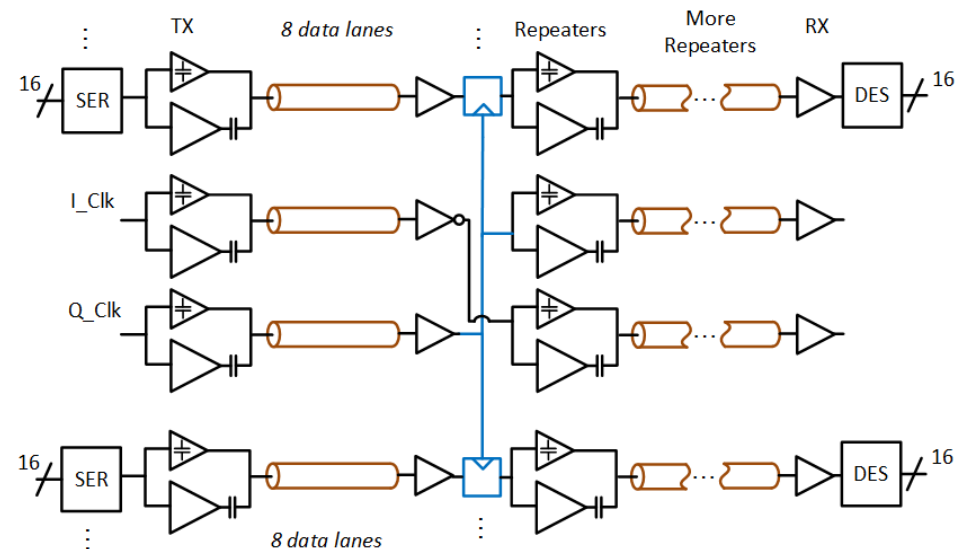
# Repeater Structure

- Amplifier
  - Linear amplifier is preferred for best delay matching between data and clock lanes
- Sampler
  - Two latch chains with DDR clocks
- Driver
  - Pre-emphasis driver + DC driver
  - Simplest way to equalize the channel



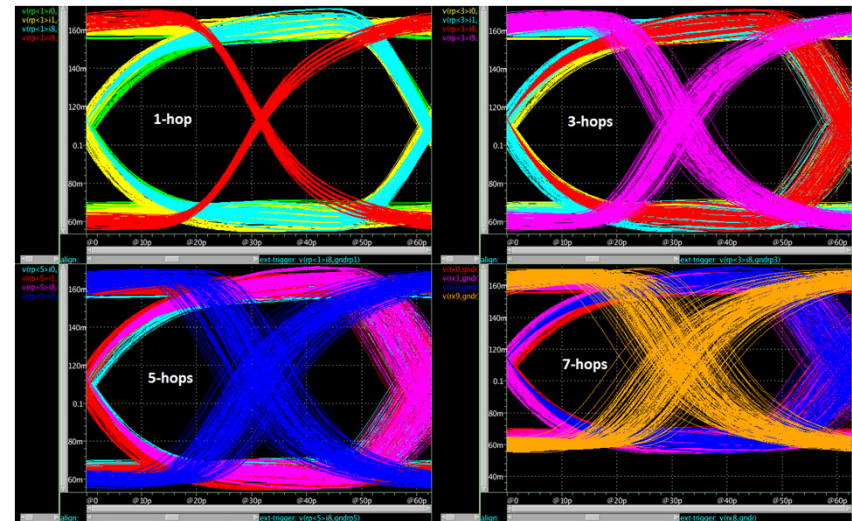
# Quadrature Clocking

- Alternating I/Q clocks
  - Sampling clocks in all repeaters come from the same clock source at the transmitter (TX).
  - Alternate I clock and Q clock in each repeater.
  - Timing margin is guaranteed for all repeaters, as long as the quadrature clocking quality is still reliable.



## Cross-talk Accumulation in Clocks

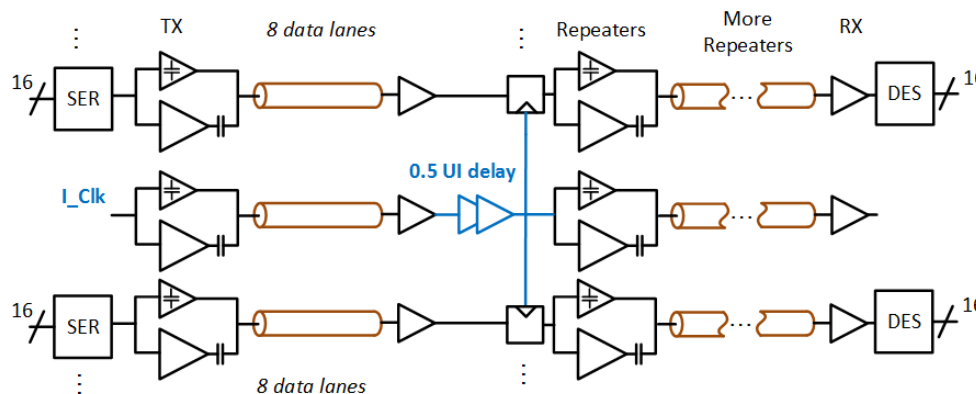
- Clock distribution is the key factor
  - Variations in clock signals will accumulate through the link.
  - Data lanes Cross-talk is the source of major interference to clocks.
  - There's a limit to the maximum distribution distance (i.e. channel length & number of repeaters) when I- and Q-clocks are not re-synthesized after the TX.



Eye diagrams of data and clock inputs at different repeater stages

## Other Clocking Methods

- I-clock only structure
  - Generate the  $\sim 0.5UI$  sampling margin locally, suffer local variations but will not accumulate, higher risk over process corners
- Pseudo-differential clocking



## Power Supply Noise Impacts

- Noise locality
  - For single-ended signaling, different voltage variations at neighboring repeaters may cause common-mode mismatch and increase jitter.
- Noise amplitude
  - Supply noise with large amplitude will cause offset accumulation, especially in clocks. Higher noise amplitude reduces the distance the global signaling can reach.
- Noise frequency
  - Normally, the frequency of noise caused by logic circuits is obviously slower than data rate in high-speed serial-link. If it's not the case, we will start to lose the delay matching capability of source-synchronous clocking, and get higher BER.

## Power Supply Noise Impacts (cont.)

- Experimental results
  - Example: 510MHz sinusoidal supply noise
  - Higher noise amplitude causes the data link to fail earlier
  - More noise patterns are explored in real applications

Vnpp/Rate	13Gb/s	14Gb/s	15Gb/s	16Gb/s	17Gb/s	18Gb/s	19Gb/s	20Gb/s
150mV	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass
200mV	Pass	Pass	Pass	Pass	Pass	Pass	6	4
250mV	Pass	Pass	Pass	Pass	Pass	6	3	3
300mV	Pass	Pass	Pass	Pass	4	3	1	1
350mV	Pass	6	3	3	3	1	1	1
400mV	6	3	3	1	1	0	0	0

On-chip data link performance at various data rates and VDD noise amplitudes  
(Totally 7 hops, 28nm technology, 900mV supply)

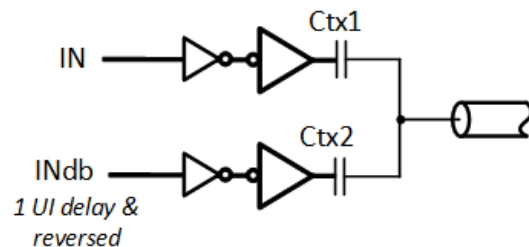


## Circuit Design Considerations

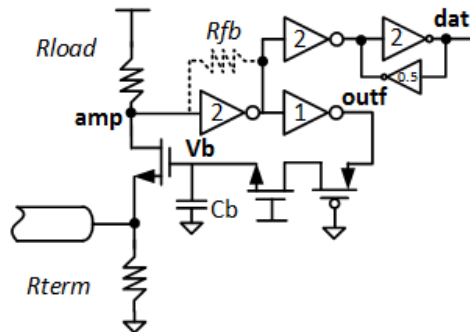
- Requirements: simple and reliable!
  - The tight power budget demands the simplest circuit solutions. But the circuit still needs to survive all process-voltage-temperature (PVT) variations.
- Some challenges and recent solutions:
  - Low swing signal generation and DC de-coupling: Charge-pump style driver [J.Poulton, ISSCC & JSSC 2013]
  - PVT variations: Amplifier with offset tuning (i.e. voltage mismatch compensation)
  - Design delay-matched clock & data paths at Tx & Rx ... include delay-trim for each data lane to align them with clocks (i.e. timing mismatch compensation).

## Circuit Design Considerations (cont.)

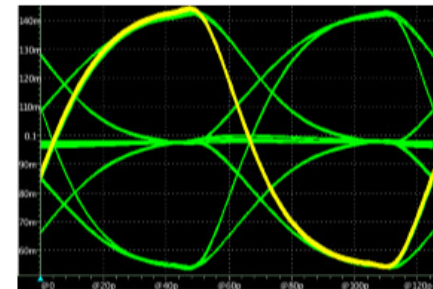
- Another method: Pulse-mode signaling
  - AC drivers only, return to common-mode voltage after the 1<sup>st</sup> transition bit.
  - Pros: Intrinsically DC de-coupled, Saves overhead of DC driver, No offset calibration needed, and VDD adaptive common-mode
  - Cons: risk of error propagation... better for “busy” data



(a) Pulse-mode driver



(b) Self-biased amplifier



(c) Eye diagrams of waveforms

## Other Possibilities

- Current mode signaling
  - The given examples in this talk are all based on voltage mode (because it's simple). But some studies for current mode have also been done.
  - Current mode signaling tends to have lower cross-talk at about same driving capability, however, it requires higher voltage headroom for current source.
- Differential signaling
  - When space margin among power grid is larger, differential signaling could be a better choice, because the cross-talk is much lower with twisted diff-channels.
  - Concerns: power and offset tuning

## Conclusion

- High-speed low-power serial-link can be a good solution for on-chip global signaling in future SoC products.
- Techniques for multi-hop serial-link, source-synchronous clocking, high-level thick metal channels and low-energy equalization show promising potential.