A Switching Linear Regulator Based on a Fast-Self-Clocked Comparator with Very Low Probability of Meta-stability and a Parallel Analog Ripple Control Module

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***Abstract*—Point of load regulators, with fast response to load transients, are becoming critical components in low power systems. Linear regulators are an area-efficient way to implement fast-response regulation as they require only the transistors and capacitors available in any standard CMOS process. This paper presents a switching linear regulator with a comparator that samples the difference between the regulated voltage and the reference (error) at 4GHz. The comparator uses a novel self-clocking scheme to achieve extremely low probability of meta-stability, even at very high clock frequency. In fast transient mode, the regulator achieves zero droop when the load current steps from $< 1mA$ to $170mA$ in 100ps. A digital ripple control mechanism, and an analog ripple control module work together to reduce the ripple on the regulated output. The regulator, fabricated in TSMC's 16nm finFET technology, achieves a peak current efficiency of 97.6% when operating at 4GHz.**

I. Introduction

Fully integrated on-die voltage regulators are becoming more and more important in systems where low power dissipation is crucial. Fine grained dynamic voltage scaling [1], variation mitigation through supply voltage tuning [2], supply voltage droop/overshoot reduction during fast load transients [3] and other such applications have necessitated the design of voltage regulators close to the point of load. Even though [4] offers the required performance, area constraints due to cost and system size considerations give linear regulators a distinct advantage over other type of regulators.

A fully integrated regulator, apart from being area efficient, should also have fast load transient response, high efficiency, stable control, low ripple and re-configurability so that it can be re-used across different projects and system implementations with varied requirements. In this paper, we present a fully integrated switching linear regulator to meet all the above system requirements. Fast transient response is achieved by sampling the error between the reference and the regulated voltage at very high frequency. High efficiency is achieved by using a positive-feedback-based clocked comparator with no static power dissipation. The probability of meta-stability is greatly reduced by using a novel self-clocking mechanism in the clocked comparator. Digital and analog ripple control mechanisms limit the ripple to a low value. The regulator is highly re-configurable and can be optimized to meet the specifications imposed by the system design. The regulator presented in this paper provides regulated voltage to a ground-reference signaling (GRS) transceiver [2] where the desired supply voltage is varied to compensate for process and temperature variations. The regulator supports transients as large as 170mA in 100ps that occur when the GRS transceiver transitions from idle to full functional mode.

II. Switching linear regulator architecture

Our regulator, shown in Figure 1, uses lower-bound hysteretic control [5] with *constant* ON-time. A high speed

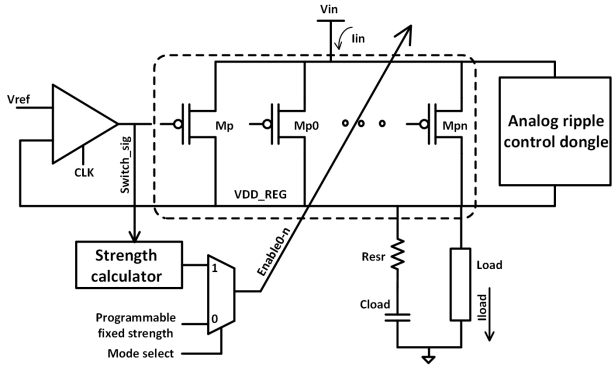

Fig. 1: Top level regulator architecture

positive feedback comparator compares the reference voltage Vref with the regulated voltage VDD_REG. When VDD_REG is lower than Vref, the controller turns ON the PMOS power switches for a fixed 1-cycle interval to charge the decoupling capacitors. The regulator has two modes of operation. In the ripple control mode, a secondary slow loop is used to adapt the size of PMOS power switches based on the load current to further reduce the ripple at low load. In the fast-transient mode, the regulator can instantaneously respond to sudden load changes with minimal droop. An independent analog ripple control module of variable strength responds to high frequency ripple by generating an opposite current to cancel the ripple.

A. Self-clocking comparator

The ripple on VDD_REG and the load transient response of the regulator are determined by how fast the regulator detects the difference between VDD_REG and Vref. To keep ripple low, the comparator must be clocked at very high frequencies. However, high frequency clocking exacerbates the problem of meta-stability, since the regulator loop forces difference between VDD_REG and Vref to be small, increasing the chance of meta-stable behavior, which leads to higher noise levels.Other work [6] proposes a method in which a detector circuit determines when the comparator has been stuck in a meta-stable state for a pre-determined time and returns the detector to its pre-charge state. However, dedicated circuitry is required to measure the comparator's latency, which increases system complexity.

Figure 2 shows our self-clocked comparator design, in which meta-stability is resolved by embedding the comparator in a loop that generates the clock. The comparator transitions from evaluate phase to pre-charge phase only when the cross-coupled nodes OUTP/OUTN of the comparator are sufficiently separated so that it is guaranteed that the positive feedback action can take them further to rails. When the difference

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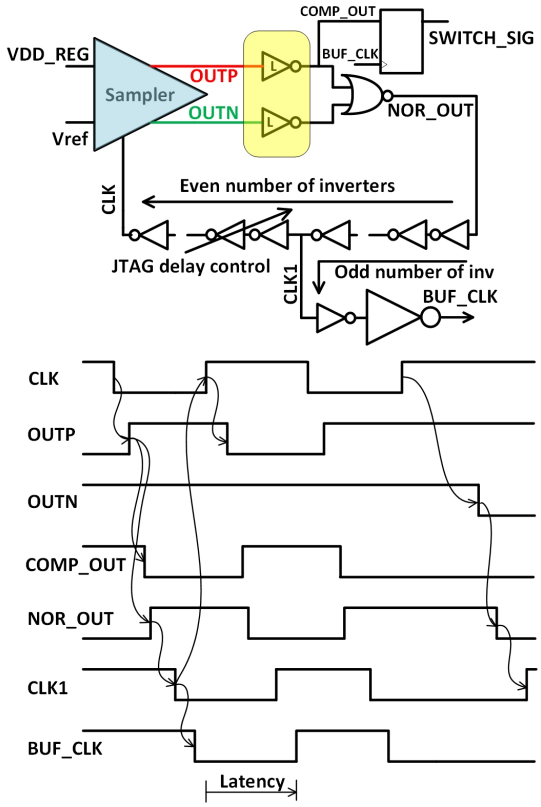
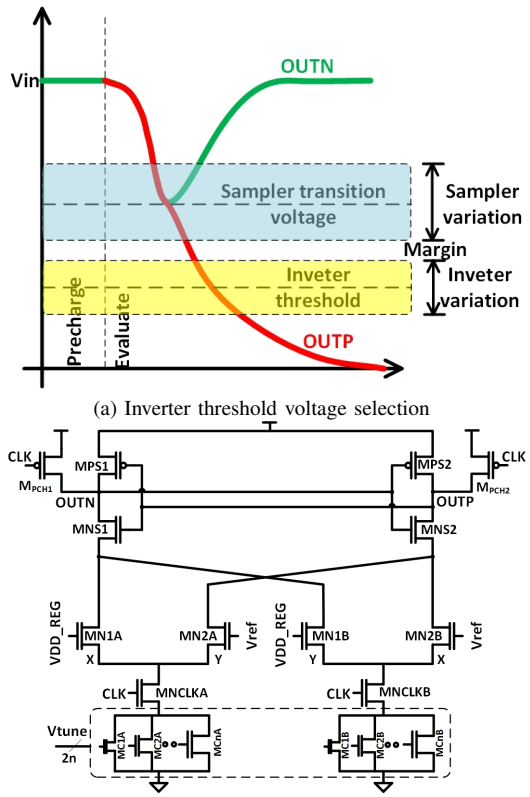


Fig. 2: Self-clocking comparator and its voltage waveform



(a) Inverter threshold voltage selection

(b) Comparator with offset cancellation

Fig. 3: Skewed inverter threshold and master stage of the clocked comparator

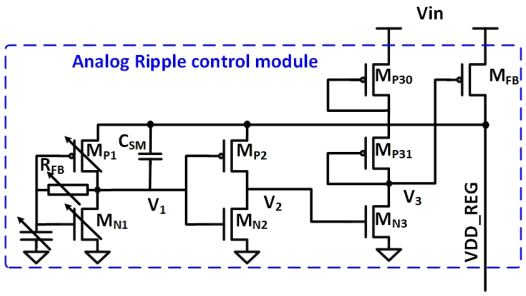
between VDD_REG and Vref is small, the comparator stays longer in the evaluate phase; when the difference is large, the comparator nodes resolve faster. On the other hand, the pre-charge phase is determined by pre-charge strength and the loop latency, independent of comparator voltage input. From a regulator point of view, when VDD_REG is nearly equal to Vref, nothing needs to be done, and the clock can be slowed down without affecting output regulation. When there is difference between VDD_REG and Vref is large, the comparison completes faster, the frequency of clock increases, and the regulator responds quickly to the output error. The separation of the OUTP/OUTN nodes is detected by skewed inverters following the comparator. The skewed inverter outputs flip only when one of the OUTP/OUTN nodes goes below its low threshold voltage. The threshold voltage is chosen such that the $\pm 6\sigma$ variation in inverter threshold voltage is separated from the $\pm 6\sigma$ variation in comparator meta-stable voltage by 100mV, as shown in Figure 3a. A programmable delay chain in the clock feedback loop allows adjustment of the clock frequency. The self clocking scheme also reduces by a half-cycle the latency in flopping the comparator output, by virtue of knowing the exact relationship between the clock edge and decision time of comparator. The accuracy of the regulator is affected by transistor-variation-induced comparator offset; Figure 3b shows the comparator offset cancellation technique implemented by steering unequal current in the two branches, A and B, of the differential comparator. The transistors in each of the differential pairs A and B are skewed in size, with $X > Y$, so each pair has a built-in offset, but of opposite sign. Offset can then be removed by setting a digital correction code on Vtune. To achieve maximum frequency of operation, all the transistors of either MCnA or MCnB group are ON and a subset of the transistors of the other group are appropriately turned OFF to cancel offset.

B. Analog ripple control

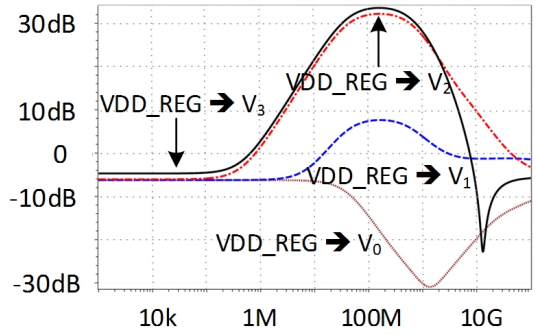
An analog ripple control module used to cancel the high frequency component of the ripple is shown in Figure 4a. It includes a resistive feedback inverter with shunt capacitor, followed by an inverter, level shifter and PMOS header in parallel with the switching linear regulator. It compares the VDD_REG with its RC filtered version and generates the voltage V_1. V_1 is further amplified (V_2) and level shifted (V_3) to control device M_{FB}. The open loop high frequency (hundred MHz range) gain is high while the low frequency gain is 0.5 as shown in Figure 4b, such that the high frequency noise on VDD_REG is reduced when the loop is closed, with little disturbance of the DC operating point if the DC load current is more than the DC current of M_{FB}. On the other hand, if the DC load current is small, VDD_REG could be pulled higher than V_ref by the module. To keep VDD_REG constant across different load scenarios, the strength of the software-programmable M_{N1} can be adjusted so that the DC current thru M_{FB} is zero, allowing the module mainly to cancel droop (not ripple) on VDD_REG.

C. Digital ripple control

A secondary control loop is used to reduce ripple by adjusting the PMOS switch size based on the load current.



(a) Analog ripple control module



(b) Gain variation at different nodes

Fig. 4: Analog ripple control module operation

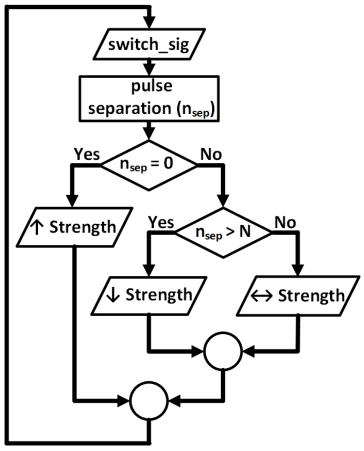


Fig. 5: Digital ripple control algorithm

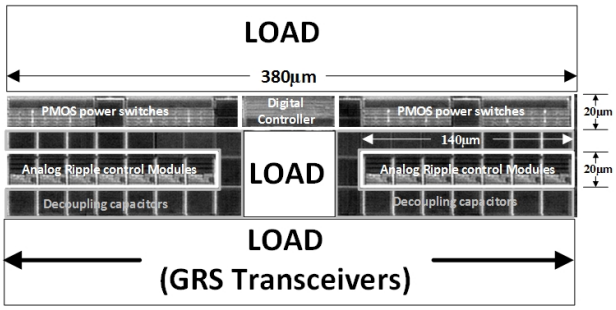


Fig. 6: Die-photo of the testchip

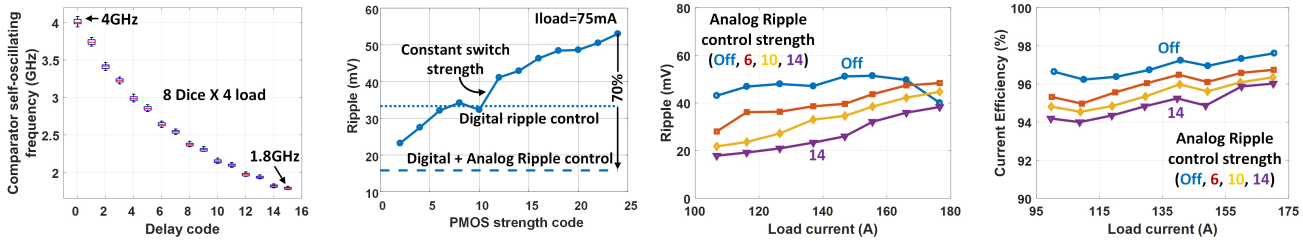
The separation between the PMOS switching pulses is measured [7], and this measurement gives an indirect estimate of the load current. The switch size is increased if pulses are spaced close to each other and decreased if pulses are far apart as shown in the flowchart in Figure 5. The switch is divided into 24 equal sized segments and physically placed such that the load current is kept uniformly distributed along the entire regulator when the switch strength is varied. This ripple control loop is slow in response and can result in droop in case of a large load transient. Alternatively, the ripple control loop can be disabled and a fixed switch strength code can be programmed to support the maximum load current. This fast-transient mode significantly reduces the droop in comparison with the ripple control mode, at the expense of additional ripple at low load currents. The regulator design is software programmable; various modes can be selected, and the analog ripple control module can be turned off, for higher energy efficiency at the cost of more noise.

The regulator, fabricated in TSMC 16nm FinFET technology, supports a maximum load current of 170mA at $0.78V$ from a 1V input voltage. The total active area is $0.0138mm^2$ as shown in Figure 6. The area occupied by the PMOS switches and the digital control logic is $0.0076mm^2$, and the area of the analog ripple control modules is $0.0056mm^2$, including the feedback resistor and shunt capacitor. The rectangular layout was chosen to accommodate the GRS transceiver layout placed above and below the regulator. There is $2.7nF$ of decoupling capacitance on the VDD_REG output node and $1.2nF$ on the input voltage node made of MOS-caps and MOM-caps stacked one above the other (not shown in die photo).

III. Measurement Results

Figure 7a shows variation of comparator self clocking frequency from 4GHz to 1.8GHz vs. programmable delay code for 8 test-chips each under 4 different load conditions. The solid line in Figure 7b shows the ripple when the ripple control loop is disabled, and a fixed switch strength is programmed for 75mA load current. 53mV ripple is measured on VDD_REG when maximum switch strength is enabled. The dotted line shows the ripple when only digital ripple control mode is turned ON. The dashed line shows ripple when the analog ripple control module is also enabled, achieving a ripple of only 15.8mV. This is a 70% reduction in ripple in comparison with the maximum strength case. Figure 7c shows the ripple on VDD_REG when the load current is varied for different analog ripple control module strengths. Measurement results show increase in ripple cancellation with increasing strength of the analog ripple control module. The corresponding current efficiency plot is shown in Figure 7d. The regulator achieves a maximum current efficiency of 97.6% at 785mV VDD_REG and 170mA load current with all the analog ripple control modules turned OFF. The current efficiency reduces to 96% when maximum analog ripple control strength is enabled.

The load transient response of the regulator for the low load to high load transition for different modes of operation is shown in Figure 8. In these tests, the load current steps from $< 1mA$ to 170mA in 100ps. When only digital ripple control is enabled, ripple is minimum at low load currents, although the load transient results in a droop of 48mV. In fast transient mode, the load transient does not result in any droop. Alternatively, the analog ripple control module, along



(a) Variation of self-clocking frequency (b) Ripple in different modes (c) Ripple variation (d) Current efficiency

Fig. 7: Characteristics of the switching linear regulator

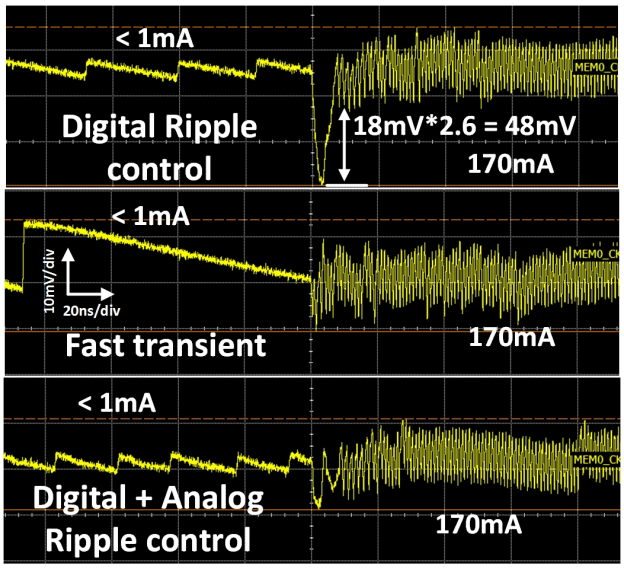


Fig. 8: Load transient response of the regulator for load transition from $< 1mA$ to 170mA in 100ps for different modes

	[8] 2017	[9] 2017	This work	
			Without analog ripple control	With analog ripple control
Process	65nm	65nm	16nm FF	16nm FF
Active area(mm^2)	0.023	0.03	0.0076	0.0132
Control	Digital SAR/PWM/ PD	Digital + analog assist	Digital Switching	Digital + analog ripple control
Vin(V)	0.5-1	0.5-1	0.9-1.05	
Vout(V)	0.3-0.45	0.45-0.95	0.53-0.95	
Max load(mA)	2	12	170	
C_L(nF)	0.4	0	2.7	
F_s max (MHz)	240	10	4000	
Load step (mA/ns)	1.1	10	1700	
Vdroop (V)	40	105	48 for dig. ripple cont. 0 for other cases	
Settling time(ns)	100	> 1000	8 for dig. ripple cont. 0 for other cases	

TABLE I: Comparison with most recent similar work

with digital ripple control, can be configured to reduce droop and yield results similar to the fast transient mode.

Table I shows the table of comparison with other recently published work. Our linear regulator handles much faster and larger load transients with less droop than the other implementations even when the slow ripple control mode is turned ON. This is due to the very high sampling frequency of the comparator ($> 10X$ compared to [8]), possible thanks to the low probability of meta-stability in the self-clocked comparator design.

IV. Conclusion

In this paper, we have presented a switching linear regulator with a very high frequency clocked comparator. The comparator uses a novel self-clocking technique to reduce the probability of meta-stability to extremely low value even with high clock frequency. The high sampling frequency enables the regulator to have an ultra-fast load transient response, as shown by the measurement results, where a zero droop on regulated voltage is observed for load transients as large as 1.7A/ns. In spite of the high sampling frequency, the regulator has a maximum current efficiency of 97.6%. Analog and digital ripple control mechanisms reduce ripple by 70% compared to the case when these are OFF. The regulator is highly reconfigurable, making it suitable to be optimized to meet different system requirements.

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